ated by the operator of the design flow, or from other sources. Design structure **920** comprises an embodiment of the invention as shown in FIG. **9**, FIG. **13**, FIG. **16** or FIG. **17**/**18** in the form of schematics or HDL, a hardware-description language (e.g., Verilog, VHDL, C, etc.). Design structure **920** may be contained on one or more machine readable medium. For example, design structure **920** may be a text file or a graphical representation of an embodiment of the invention as shown in FIG. **9**, FIG. **13**, FIG. **16** or FIG. **17**/**18**. Design process **910** preferably synthesizes (or translates) an embodiment of the invention as shown in FIG. **9**, FIG. **13**, FIG. **16** or FIG. **17** into a netlist **980**, where netlist **980** is, for example, a list of wires, transistors, logic gates, control circuits, I/O, models, etc. that describes the connections to other elements and circuits in an integrated circuit design and recorded on at least one of machine readable medium. This may be an iterative process in which netlist **980** is resynthesized one or more times depending on design specifications and parameters for the circuit.

Design process **910** may include using a variety of inputs; for example, inputs from library elements **930** which may house a set of commonly used elements, circuits, and devices, including models, layouts, and symbolic representations, for a given manufacturing technology (e.g., different technology nodes, 32 nm, 45 nm, 90 nm, etc.), design specifications **940**, characterization data **950**, verification data **960**, design rules **970**, and test data files **985** (which may include test patterns and other testing information). Design process **910** may further include, for example, standard circuit design processes such as timing analysis, verification, design rule checking, place and route operations, etc. One of ordinary skill in the art of integrated circuit design can appreciate the extent of possible electronic design automation tools and applications used in design process **910** without deviating from the scope and spirit of the invention. The design structure of the invention is not limited to any specific design flow.

Design process **910** preferably translates an embodiment of the invention as shown in FIG. **9**, FIG. **13**, FIG. **16** or FIG. **17**/**18**, along with any additional integrated circuit design or data (if applicable), into a second design structure **990**. Design structure **990** resides on a storage medium in a data format used for the exchange of layout data of integrated circuits and/or symbolic data format (e.g. information stored in a GDSII (GDS2), GL1, OASIS, map files, or any other suitable format for storing such design structures). Design structure **990** may comprise information such as, for example, symbolic data, map files, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, data for routing through the manufacturing line, and any other data required by a semiconductor manufacturer to produce an embodiment of the invention as shown in FIG. **9**, FIG. **13**, FIG. **16** or FIG. **17**/**18**. Design structure **990** may then proceed to a stage **995** where, for example, design structure **990**: proceeds to tape-out, is released to manufacturing, is released to a mask house, is sent to another design house, is sent back to the customer, etc.

Embodiments of the invention are illustrative of the invention rather than limiting of the invention. Revisions or modifications may be made to methods, materials, structures or dimensions of a CMOS pixel sensor cell in accordance with the embodiments while still providing a pixel sensor cell (which need not necessarily be a CMOS pixel sensor cell), method for fabrication thereof or design structure for fabrication thereof in accordance with the invention, further in accordance with the accompanying claims.

What is claimed is:

1. A pixel sensor cell comprising:

a photoactive region located within a first semiconductor layer, wherein the first semiconductor layer is located a second semiconductor layer;

a transistor located partially within the second semiconductor layer, wherein the second semiconductor layer is located a carrier substrate;

a light blocking layer located interposed between the first semiconductor layer and the second semiconductor layer and shielding the transistor from back side illumination; and

a contact region comprised of a semiconductor material extending through the light blocking layer, wherein the contact region contacts the first semiconductor layer and the second semiconductor layer.

2. The pixel sensor cell of claim **1**, further comprising a first transistor located within the first semiconductor layer and not shielded by the light blocking layer.

3. The pixel sensor cell of claim **2**, wherein the light blocking layer comprises a gate for the first transistor.

4. The pixel sensor cell of claim **1**, further comprising a floating diffusion region that is located within the second semiconductor layer and shielded by the light blocking layer.

5. The pixel sensor cell of claim **1**,

wherein the contact region comprises a first p-dopant concentration from about 1×10^{19} to about 5×10^{20} p-dopant atoms per cubic centimeter,

wherein the photoactive region comprises an n-dopant concentration from about 1×10^{15} to about 1×10^{17} n-dopant atoms per cubic centimeter, and

wherein the first semiconductor layer comprises a second p-dopant concentration from about 1×10^{13} to about 1×10^{16} p-dopant atoms per cubic centimeter.

6. A design structure embodied in a non-transitory computer readable storage medium, which when being executed by a computer implements a method for designing, manufacturing, or testing an integrated circuit, the design structure comprising:

a pixel sensor cell comprising:

a photoactive region located within a first semiconductor layer, wherein the first semiconductor layer is located on a second semiconductor layer;

a transistor located partially within the second semiconductor layer, wherein the second semiconductor layer is located on a carrier substrate;

a light blocking layer located interposed between the first semiconductor layer and the second semiconductor layer and shielding the transistor from back side illumination; and

a contact region comprised of a semiconductor material extending through the light blocking layer, wherein the contact region contacts the first semiconductor layer and the second semiconductor layer.

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